

Abstract

A circuit arrangement and technique are provided for passing N-bit digital data using an M-bit datapath, M being less than N. A plurality of N-bit words is arranged for transfer in two portions. A first portion of each of the plurality of words is transferred in M-bit groups. At least one other bit group is transferred, including bits from the second portions of at least two of the plurality of words. After transfer, each first portion is reassembled with a corresponding second portion into respective N-bit words. The digital data is arranged for transfer at one rate, and transferred at a second rate at least as fast as the first rate. In one embodiment, X words of data are transferred from one storage element while another X words are arranged for transfer in another storage element. In a more particular embodiment, 10-bit data is passed over a standard 8-bit digital visual interface.

10005942 10801